**CDAC Feb 2015**

**LAB 5**

Q1. IP Core Generator

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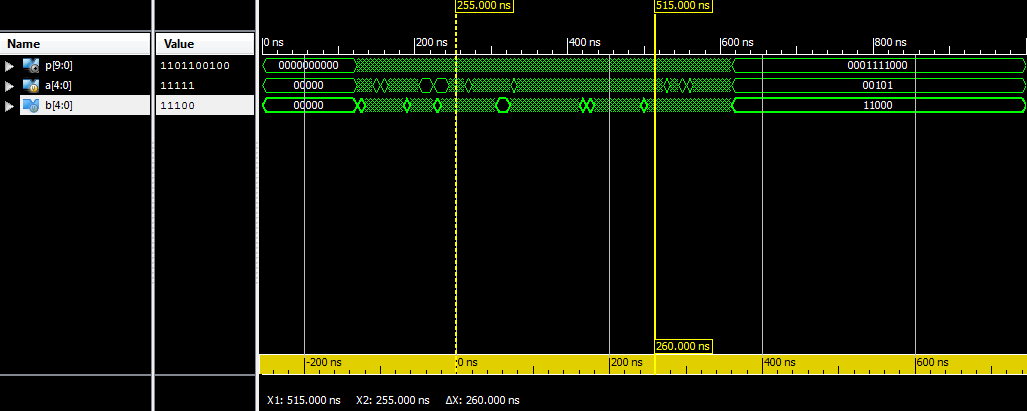
**IP Core Generator**

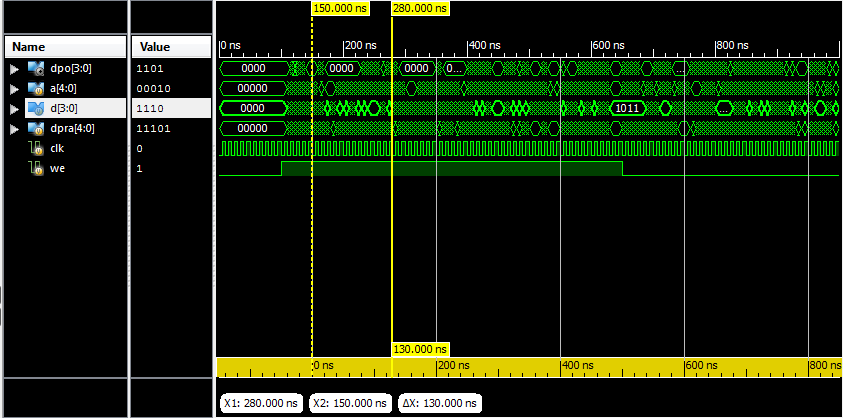
# Design Approach:

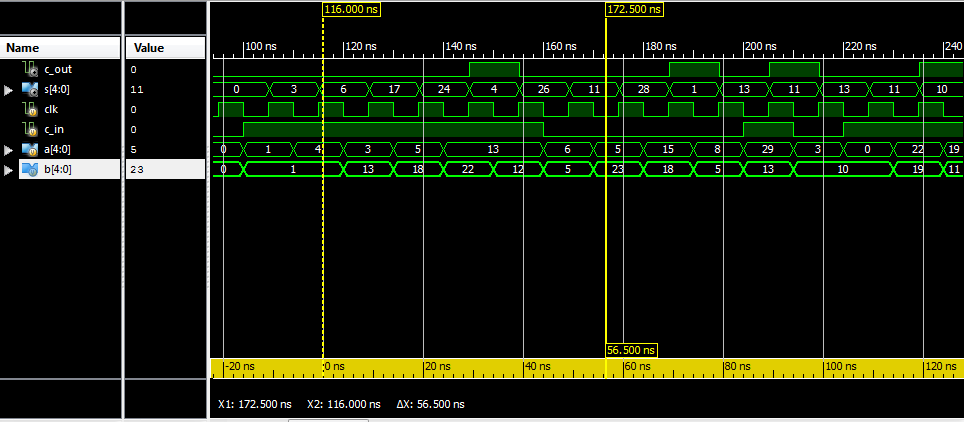
IP cores are blocks or modules that have been designed and tested to perform a specific function such as processors, Ethernet interfaces and RAM controllers. Soft IP cores are in the form of HDL and typically have IP license associated with them. These IP cores are focused to perform the best outcome for any requirement from the board. Hard cores are synthesized blocks that can be instantiated, placed in your design. We have designed the requirement using the intellectual property of the same design available with Xilinx ISE.

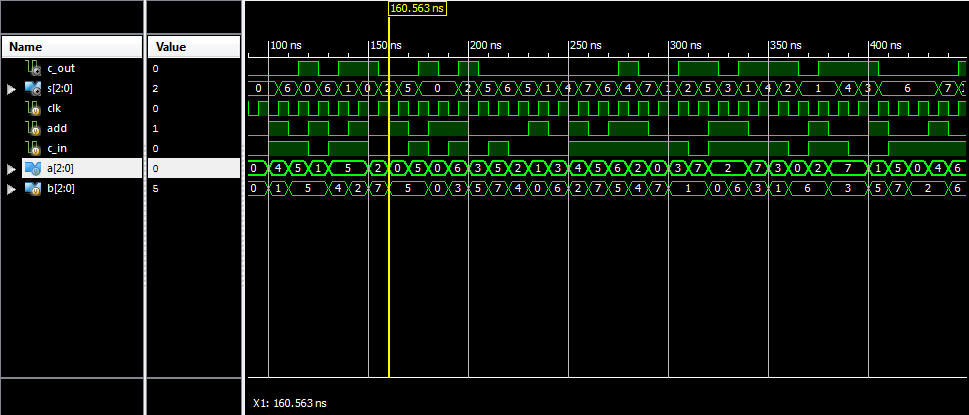
**Synthesis:**

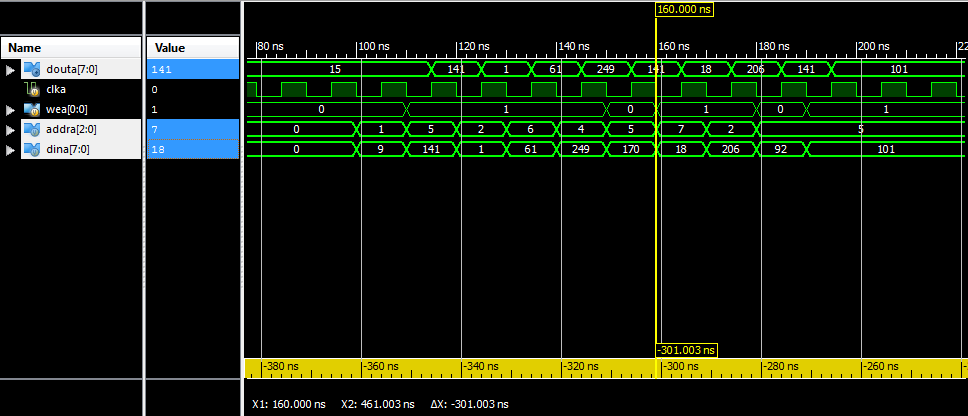
1. Simulation Waveform Result



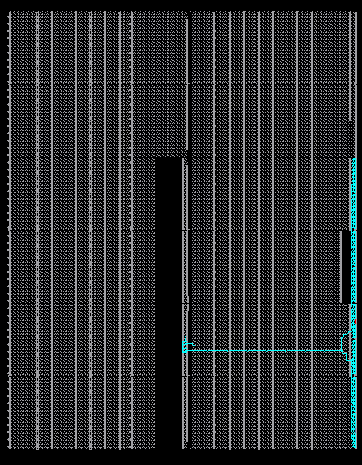
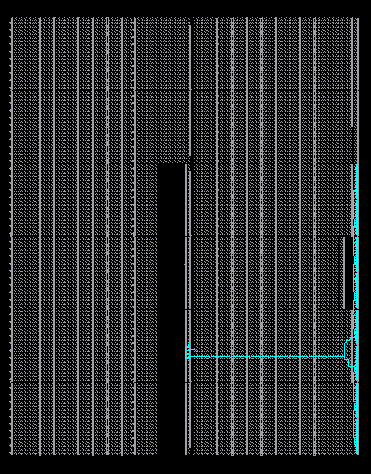








1. FPGA Editor Outputs

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**Error:**

None

**Verified by:**

Dharamvir Chundawat (150240133007)